RAK3203 802.11b/g/n Wi-Fi® Series Module Data Sheet V1.0

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Content

Devices Overview

RAK3203 is an ultra-low-power, low-cost module that fully supports of major encryption modes as well as WAPI encryption mode, a Wi-Fi ® module with SDIO interface that supports 802.11b/g/n protocol. The module internally integrates RF station, RF switch, crystal oscillator and power switch circuit, enabling fast hardware design. Plus, maturely powered by WINCE, Linux and Android environment simplifies customer software design.

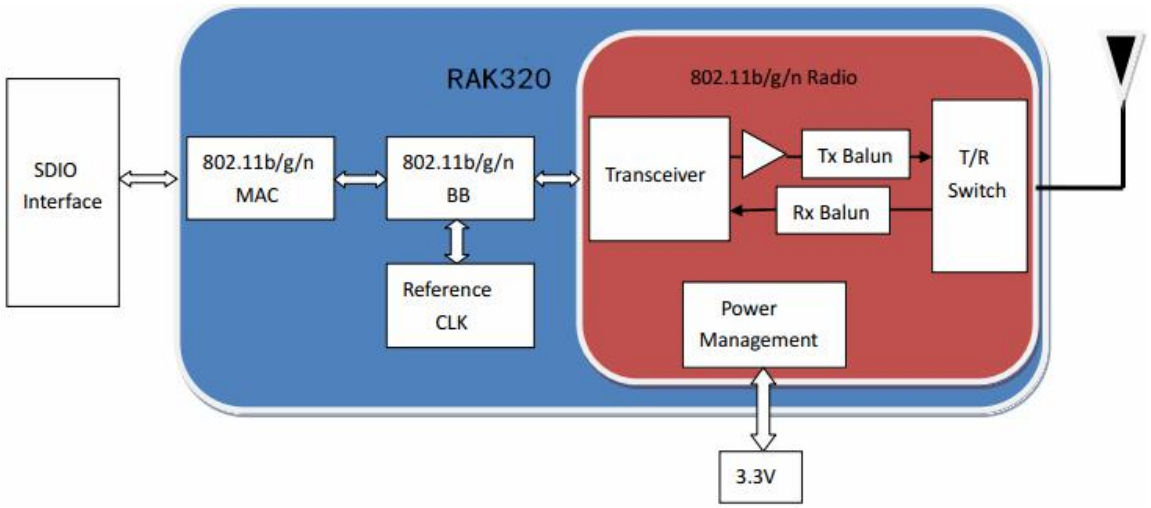
Devices Features

- Support IEEE 802.11b/g/n wireless standards, IEEE 802.11n uniflow, enabling high throughput rate
- Support SDIO 2.0 interfaces
- Support WEP, WPA/WPA2-PSK,TKIP encryption
- Infrastructure mode, Ad-Hoc mode
- Support WIFI Direct
- Completely WLAN drive under different OS, such as WINCE、Linux and Android
- Power supply: 3.14~3.46V
- Working temperature: -5~+55℃
- Package size: 16.08mm x 14.08mm x 2.2mm(**Including shield thickness**)

Key Applications

- Tablet PC
- Medical Device
- Industrial Handset
- Industrial automation and measurement
- WIFI Camera
- Internet-based Consumer electronics, like playing station

RAK 3203Series System Diagram



1 Functional Description

1.1 Host Interface

- SDIO Interface
- SDIO 1.0 & 2.0 compatible
- Support SDIO 1bit, 4bit mode
- Maximum clock frequency: 50MHz

1.2 WLAN

1.2.1 MAC

- Comply with IEEE802.11b/g/n standards
- Support WEP, WPA/WPA2-PSK, TKIP, AES encryption
- Support WAPI, business level encryption
- Support WPS-PBC

1.2.2 Baseband Processor

- Support DSSS (1, 2Mbps), CCK(1, 2, 5.5, 11Mbps), OFDM (6, 9, 12, 18, 24, 36, 48, 54Mbps), HT20 (MCS0 - MCS7)
- Adopt Orthogonal Frequency Division Multiplexing (OFDM) technology, combining with BPSK, QPSK, 16-QAM and 64-QAM
- 820.11b with CCK and DSSS modulation technology

1.2.3 Internal Frequency

- Internally integrate26MHz high-accuracy reference clock, simplifying clock circuit design

1.2.4 Power Management

- Internally integrate power management module, supporting 5 power working states: OFF state, HOST-OFF state, SLEEP state, WAKE-UP state, ON state
- Internally power supply switch: with external 3.3V main power supply only, switching to internal power management module to supply, and performing management

1.2.5 RF Circuit

- Internally integrate power amplifier, transceiver and RF switch
- Externally connect RF part to antenna through u.FL interface
- Highly integrated RF circuit greatly simplifies RF design, without need to concern the RF circuit of Wi-Fi part

2 Electrical Characteristics

2.1 Absolute Maximum

The Table 2-1 shows the absolute maximum, the Table 2-2 shows the working conditions that RAK3203 recommends. The absolute maximum is a value, exceeding which any operation would cause damage to the devices, thus it is not recommended to perform any operation above this maximum value or other values indicated in this document.

Table 2-1 absolute maximum

Symbols	Parameters	Max Value	Unit
VDD3V3	External 3.3V supply voltage	-0.3 ~ 4.0	V
3.3V IO VIH Max	When IO voltage is 3.3V, IO Max voltage	VDD+0.3	V
VIH Min	When IO voltage is 3.3V, IO Min voltage	-0.3	V
RFin	Max RF input (based on 50Ω input)	+10	dBm
Tstore	Storage ambient temperature	-40~+80	℃
ESD	ESD resistance	2000	V

2.2 Recommended Operating Parameters

Table 2-2 Recommended Operating Parameters

Symbols	Parameters	Min Value	Typical Value	Max Value	Unit
VDD3V3	External 3.3v voltage	3.14	3.3	3.46	V
$T_{ambient}$	Ambient temperature	-5		55	℃

2.3 DC Electrical Characteristics

Table 2-3 and Table 2-4 illustrate the general DC electrical characteristics under the recommended operating conditions (except special statement)

Table 2-3 general DC electrical characteristics (3.3V I/O Operating)

Symbols	Parameters		Conditions	Min Value	Typical Value	Max Value	Unit
V_{IH}	High level input			0.7xVDD			V
V_{IL}	Low level input					0.3xVDD	V
I_{IL}	Input leakage current	No pull-up, pull-down resistance	0<VIN<VDD 0<VOUT<VDD	0		-3	nA
		Pull-up	0<VIN<VDD 0<VOUT<VDD	16		48	μA
		Pull-down	0<VIN<VDD 0<VOUT<VDD	-14		-47	μA
V_{OH}	High level output		IOH=-4mA	0.9xVDD			V
			IOH=-12mA	0.9xVDD			V
V_{OL}	Low level output		IOH=4mA			0.1xVDD	V
			IOH=12mA			0.1xVDD	V

2.4 RF Electrical Characteristics

Table 2-4 illustrates RF Transmit Specifications and RF electrical characteristics of receiver specifications.

Table 2-4 RF Specifications

Main index	Characteristic parameters
Operating Frequency	2.400~2.4835 GHz
Operating Channel	11: (Ch. 1-11) – United States 13: (Ch. 1-13) – Europe 14: (Ch. 1-14) – Japan
Standards	WIFI IEEE 802.11b/g/n
Modulation	802.11b: CCK(11, 5.5Mbps), QPSK(2Mbps), BPSK(1Mbps), 802.11 g/n: OFDM
PHY data rates	802.11b: 11,5.5,2,1 Mbps 802.11g: 54,48,36,24,18,12,9,6 Mbps 802.11n: up to 150Mbps
Transmit Output Power (Tolerance: ±2.0dBm)	802.11b@11Mbps 16dBm 802.11g@6Mbps 15dBm 802.11g@54Mbps 15dBm 802.11n@(MCS 0_HT20) 14dBm 802.11n@(MCS 7_HT20) 14dBm 802.11n@(MCS 0_HT40) 13dBm 802.11n@(MCS 7_HT40) 13dBm
Receiver Sensitivity	802.11b@11Mbps -82±1dBm 802.11g@54Mbps -71±1dBm 802.11n@(MCS 7_HT20) -67±1dBm 802.11n@(MCS 7_HT40) -64±1dBm

3 AC Specification

3.1 SDIO Interface Timing Diagram

Figure 3-1 shows the SDIO interface time sequence.

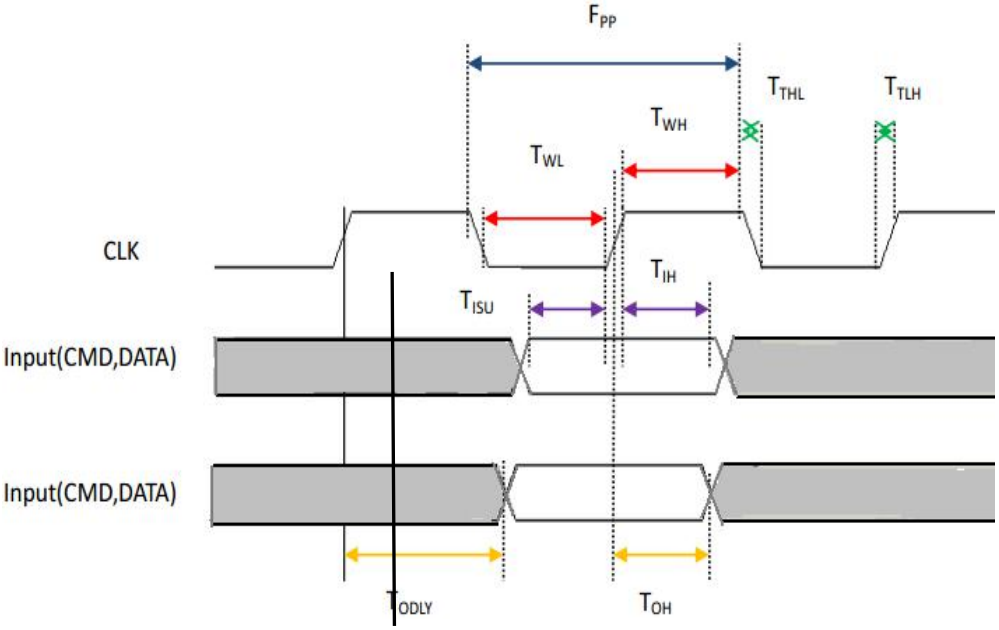


Figure 3-1 SDIO Interface Time Sequence Diagram

3.2 SDIO Interface Timing Requirement

Table 3-2 illustrates the parameter requirement under SDIO interface time sequence.

Table 3-2 SDIO Interface Timing Parameter Requirement

Symbols	Parameters	Min Value	Max Value	Unit	Note
F_{PP}	Clock frequency of data transfer	0	50	MHz	40pF≥CL
T_{WL}	Clock time in low level	7		ns	40pF≥CL
T_{WH}	Clock time in high level	7		ns	40pF≥CL
T_{TLH}	Clock time of rising edge		10	ns	40pF≥CL
T_{THL}	Clock time of falling edge		10	ns	40pF≥CL
T_{ISU}	Time of input set up	6		ns	40pF≥CL
T_{IH}	Time of input hold	2		ns	40pF≥CL
T_{OH}	Time of output maintained	2.5		ns	40pF≥CL
T_{ODLY}	Output delay in data transmission mode	0	14	ns	40pF≥CL

3.3 Reset Timing

Figure 3-2 shows the module timing when power on and power off。

Figure 3-3 shows the reset time sequence。

Table 3-3 shows the reset timing requirement range.

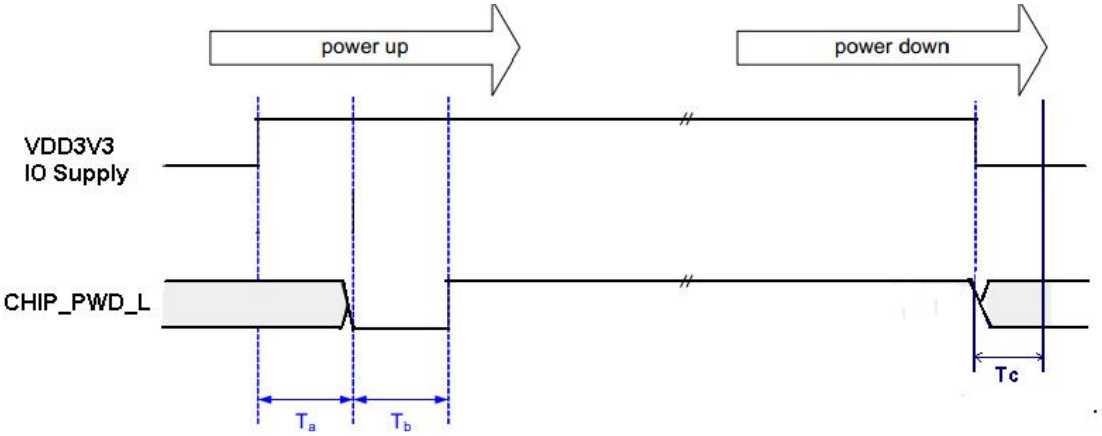


Figure 3-2Power on/Power off Time Sequence Diagram

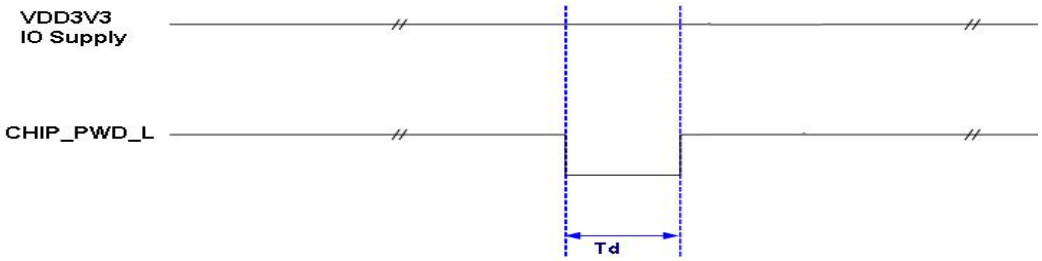


Figure 3-3Reset Time Sequence Diagram

Table 3-3Reset Timing Parameter Requirement

Symbols	Descriptions	Min Value（μS）
Ta	Time period from VDD3V3 power on to IO power effective	0
Tb	Time period from VDD3V3 effective to reset completed	5
Tc	Time period from VDD3V3 power off to reset effective	NA
Td	Reset pulse length	5

4 Pin Definition

4.1 Module Pin Assignment

Figure 4-1 shows module RAK3203 pin assignment diagram.

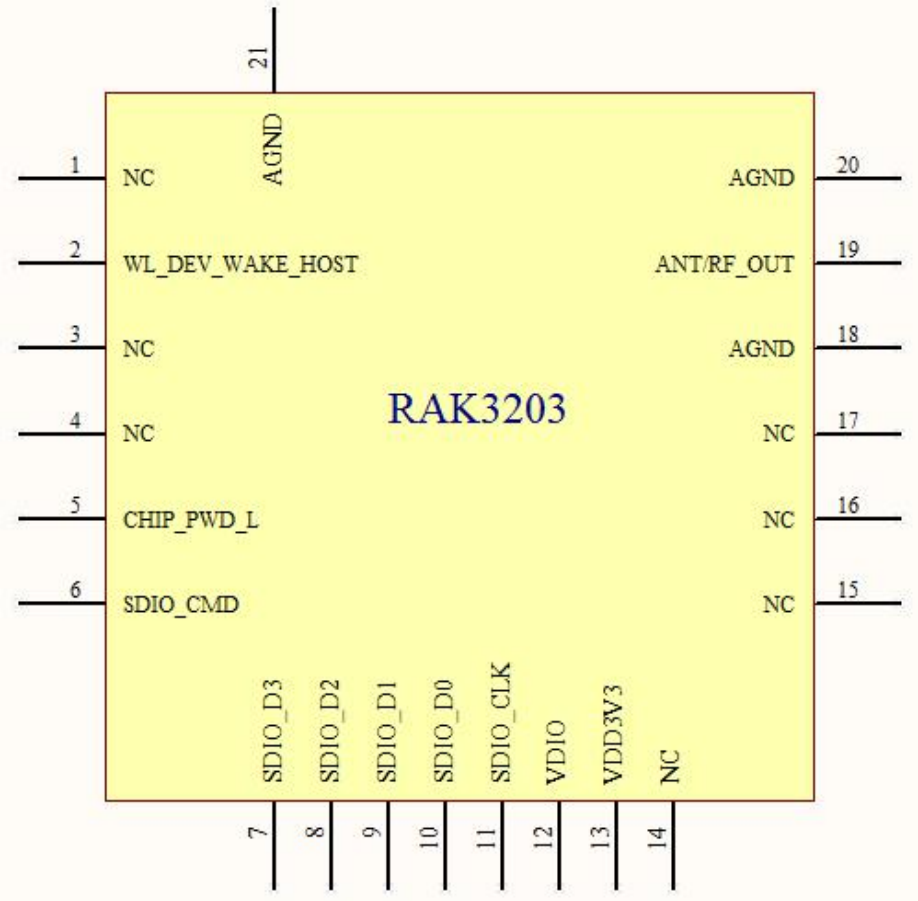


Figure 4-1 RAK3203 Pin Assignment Diagram

4.2 Module Pin Description

Table 4-1 shows module RAK3203 pin description diagram.

Table 4-1 RAK3203 Pin Description

Pin No.	Name	Description
2	WL_DEV_WAKE_HOST	Activate Wi-Fi function
5	CHIP_PWD_L	Reset module
6	SDIO_CMD	SDIO command
7	SDIO_D3	SDIO data position 3
8	SDIO_D2	SDIO data position 2
9	SDIO_D1	SDIO data position 1
10	SDIO_D0	SDIO data position 0
11	SDIO_CLK	SDIO clock line
12	VDIO	3.3V Power Supply
13	VDD3V3	3.3V Power
19	ANT/RF_OUT	Can design the on-board antenna and RF OUT
18,20,21	AGND	GND
1,3,4,14,15.16,17	NC	NC

Note:

1. Table 4-1 pin type letter explanation，P: Power I: Input O: Output IO: Bidirectional input/output; the 26th pin is the center exposed pad.
2. 19 RF output pin, can design the on-board antenna. can hung up if not use it.

5 Hardware Introduction

5.1 Top View

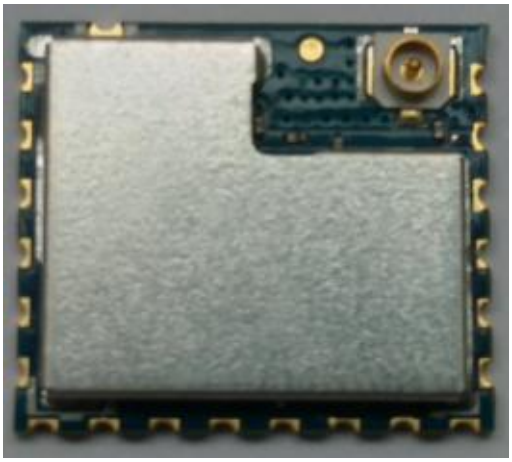


Figure 5-1 RAK3203 Top View

5.2 Bottom View

Figure 5-2 RAK3203 Bottom View

5.3 RAK3203 Recommended PCB Mechanical Size

Figure 5-3 shows the recommended PCB mechanical size (mm).

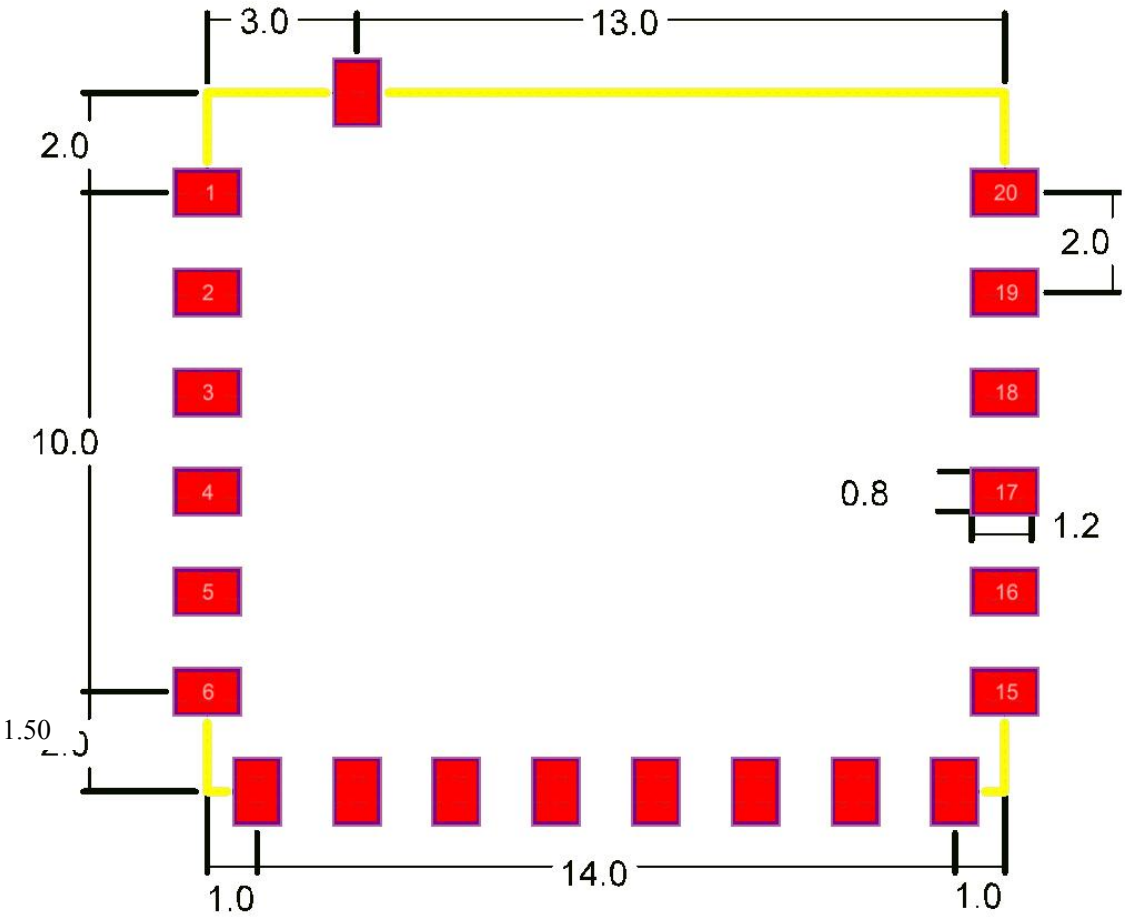


Figure 5-3 PCB Mechanical Size

6 Design Reference

6.1 Design Reference in SDIO Interface Mode

Figure 6-1 illustrates the module RAK3203 design reference diagram in SDIO interface working mode.

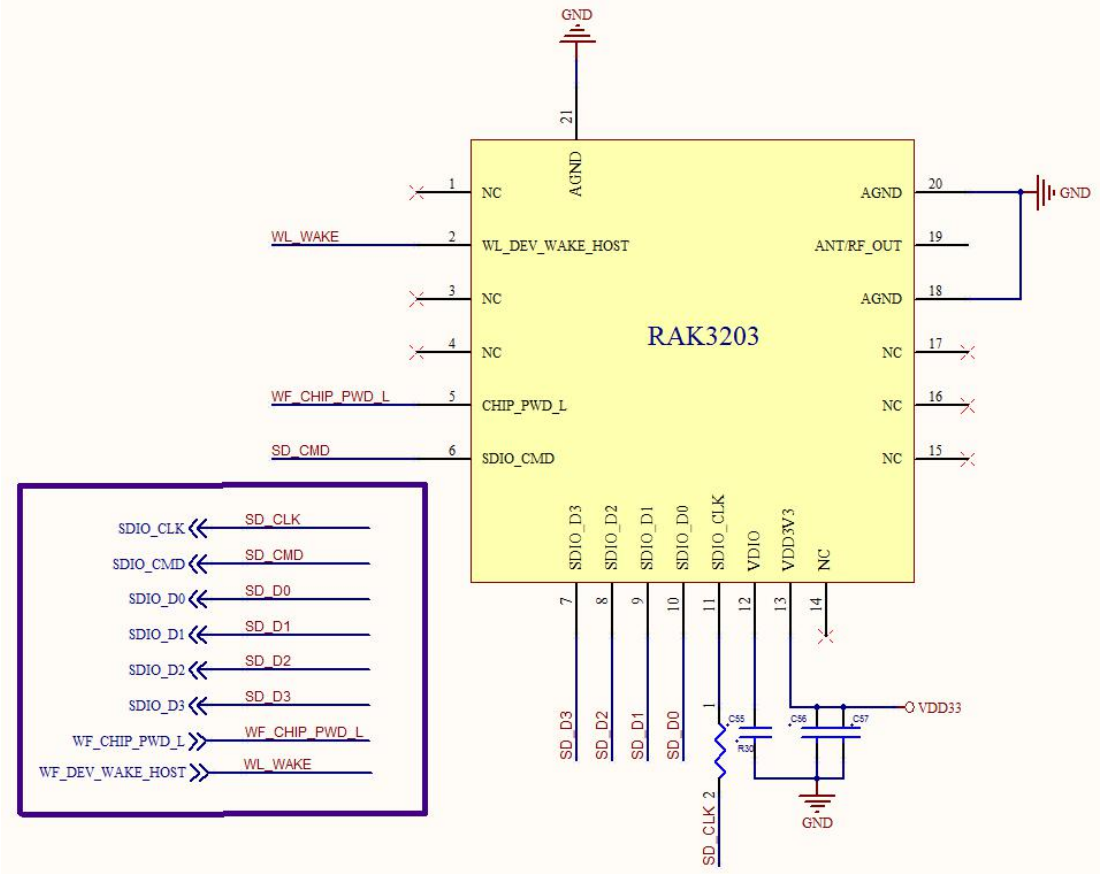


Figure 6-1 SDIO Interface Mode Diagram

Note: 19 RF output pin, can design the on-board antenna. can hung up if not use it.

7 Power Management

Table 7-1 Power Saving Mode

Working Mode	Working State	Power Consumption
Power saving	OFF	0.004mA
	HOST_OFF	0.048mA
	SLEEP	0.215mA
Continue receive (max)	54Mbps(OFDM)	86mA
Continue transmit (max)	54Mbps(OFDM)	210mA

OFF State: enter this state by directly pulling down CHIP_PWD_L pin;sleep clock is disabled in this state, no state is enabled.

HOST_OFF State: WLAN is disabled，only host interface is live, all the other parts of chip are disabled；Wake up by sending commands to host register.

SLEEP State: Only sleep clock works, Oscillator and crystal are disabled, any waking event will compulsively make a transfer from this state to WAKE-UP state.

8 Manufacturing Guidance

Figure 8-1 shows the temperature graph when manufacture by reflow soldering method.

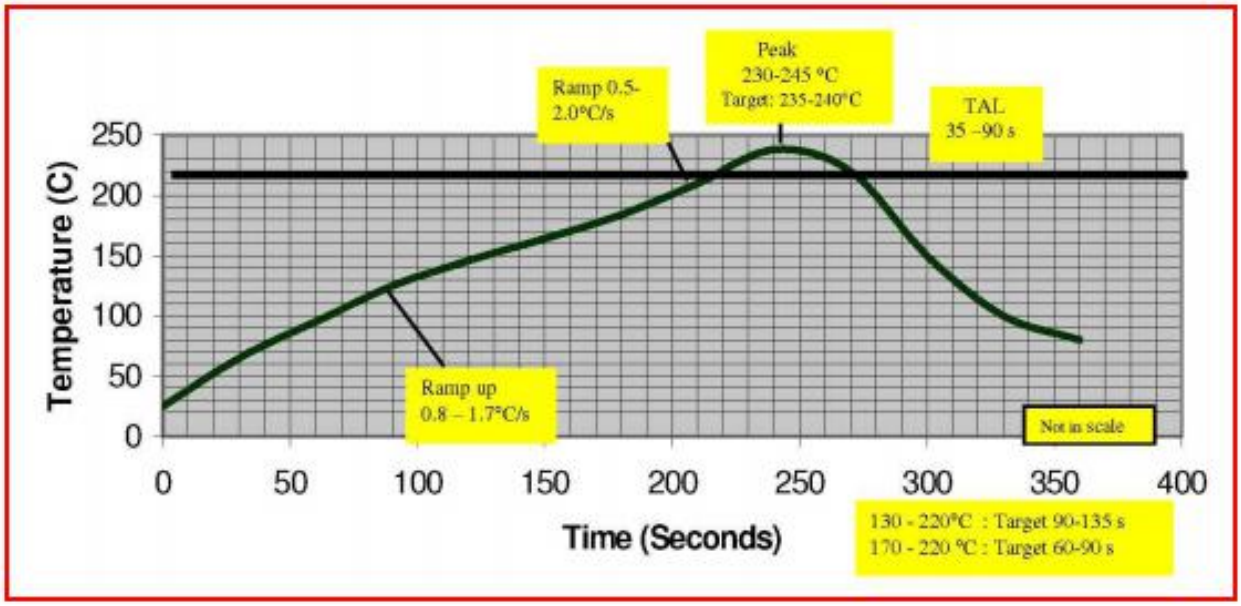


Figure 8-1 Recommended Reflow Soldering Temperature Graph

Note: as shown in the above figure, it is based on the SAC305 lead-free tin paste (3% silver, 0.5% copper). Alpha OM-338 lead-free cleaning-free flux is recommended. This figure is mainly used for guidance. The entire process time is subject to thermal pad number of assembly board and device Intensity.

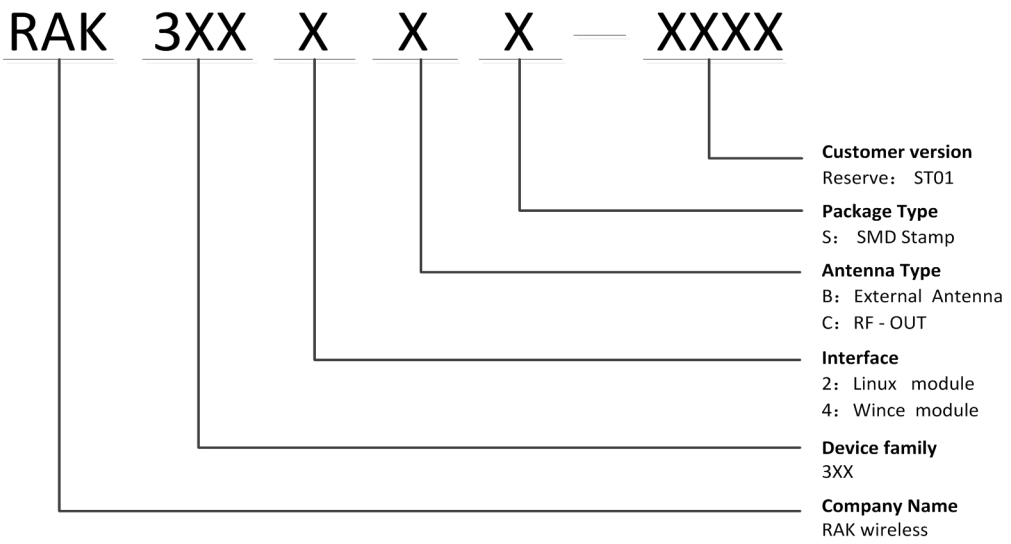
9 Order Information

9.1 Product Information

Products

P.N	Description	Single Tray Packing	Minimum Package
RAK3202BS-XXXX	Supply driver under Linux& Android OS, External Antenna	70pcs/tray	700pcs
RAK3202CS-XXXX	Supply driver under Linux & Android OS, RF-OUT	70pcs/tray	700pcs
RAK3203BS-XXXX	Supply driver under Linux & Android OS, External Antenna	70pcs/tray	700pcs
RAK3203CS-XXXX	Supply driver under Linux & Android OS, RF-OUT	70pcs/tray	700pcs
RAK3204BS-XXXX	Supply driver under WINCE OS, External Antenna	70pcs/tray	700pcs
RAK3204CS-XXXX	Supply driver under WINCE OS, RF-OUT	70pcs/tray	700pcs

9.2 Description



9.3 Others

Product Models: RAK3203(Pb Free)Tray

Weight: 0.74g/pcs

10 Sales and technical support

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11 Revision History

Revision History

Revision	Description	Date
V1.0	Documents created	2016-05-31